REMARKS

At the outset, Applicants thank the Examiner for the thorough review and consideration of the subject application. The Non-Final Office Action of January 5, 2004 has been received and its contents carefully reviewed.

In the Non-Final Office Action, the Examiner rejected claims 1-26 under 35 U.S.C. §103(a) as being anticipated by Moon (U.S. Patent No. 5,793,346) in view of Osada et al. (U.S. Patent No. 6,271,812). This rejection is traversed and reconsideration of the claims is respectfully requested in view of the following remarks.

Claim 1 is allowable over Moon in view of Osada et al. in that claim 1 recites a combination of elements including, for example, "thin film transistors defining liquid crystal cells... connected to... gate lines and... data lines... level shifting means for receiving a power supply and a ground voltage to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on and to apply a higher voltage level than the ground voltage to the gate lines upon power-off." Neither Moon nor Osada et al., singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicants respectfully submit that claims 2-8, which depend from claim 1, are also allowable over Moon in view of Osada et al.

Claim 9 is allowable over Moon in view of Osada et al. in that claim 9 recites a combination of elements including, for example, "A residual image eliminating method for a liquid crystal display device including thin film transistors connected between gate lines and data lines... the method comprising... receiving a power supply voltage and a ground voltage to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on; and applying a higher level voltage than the ground voltage to the gate lines upon power off." Neither Moon nor Osada et al., singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicants respectfully submit that claim 10, which depends from claim 9, is also allowable over Moon in view of Osada et al.

Claim 11 is allowable over Moon in view of Osada et al. in that claim 11 recites a combination of elements including, for example, "liquid crystal cells, each liquid crystal cell having a thin film transistor... a gate voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output; and a voltage enhancing device having a capacitor coupled to the output and the second voltage source, wherein when the first voltage source is turned on, the capacitor is charged and when the first voltage source is turned off, the capacitor boosts the gate off voltage at the output to be higher than a threshold voltage of the thin film transistor." Neither Moon nor Osada et al., singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicants respectfully submit that claims 12-18, which depend from claim 11, are also allowable over Moon in view of Osada et al.

Claim 19 is allowable over Moon in view of Osada et al. in that claim 19 recites a combination of elements including, for example, "liquid crystal cells, each liquid crystal cells having a thin film transistor... a gate-off voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output; and a voltage enhancing device having a capacitor coupled to the output and the second voltage source, wherein when the first voltage source is turned on, the capacitor is charged and when the first voltage source is turned off, the capacitor boosts the gate off voltage at the output to be higher than a threshold voltage of the thin film transistor." Neither Moon nor Osada et al., singly or in combination, teaches or suggests at least these features of the claimed invention. Accordingly, Applicants respectfully submit that claims 20-26, which depend from claim 19, are also allowable over Moon in view of Osada et al.

In rejecting claims 1, 9, 11, and 19, the Examiner correctly acknowledges that Moon fails to teach "how to eliminate residual images by applying a voltage level for turning off the TFT transistors upon power on." Applicants respectfully submit, however, that claims 1, 9, 11, and 19 do not generically recite a device capable of eliminating residual images by "applying a voltage level for turning off the TFT transistors upon power on," as implied by the Examiner. To reiterate, claim 1 requires, among other elements, "level shifting means for receiving a power supply voltage and a ground voltage to apply a first voltage level for turning off the thin film

transistors to the gate lines upon power-on," claim 9 requires, among other elements, "receiving a power supply voltage and a ground voltage to apply a first voltage level for turning off the thin film transistors to the gate lines upon power-on," claim 11 requires, among other elements, "liquid crystal cells, each liquid crystal cell having a thin film transistor... a gate voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output; and a voltage enhancing device having a capacitor coupled to the output and the second voltage source, wherein when the first voltage source is turned on, the capacitor is charged and when the first voltage source is turned off, the capacitor boosts the gate off voltage at the output to be higher than a threshold voltage of the thin film transistor," and claim 19 requires, among other elements, "liquid crystal cells, each liquid crystal cells having a thin film transistor... a gate-off voltage generator having a transistor connected between a first voltage source and a second voltage source to generate a gate-off voltage at an output; and a voltage enhancing device having a capacitor coupled to the output and the second voltage source, wherein when the first voltage source is turned on, the capacitor is charged and when the first voltage source is turned off, the capacitor boosts the gate off voltage at the output to be higher than a threshold voltage of the thin film transistor." Moon fails to teach or suggest the aforementioned claimed combination of elements.

To cure the Examiner's cited deficiency of Moon, the Examiner cites Osada et al. as teaching "an electroluminescent display device in which residual images stored as electric charges in pixels are eliminated... wherein the residual picture images are eliminated which the EL display panel is turned on." The Examiner then concludes that it would have been obvious to "combine Moon and Osada et al.... to achieve a display device wherein undesirable images appearing on a display screen are made invisible upon power on." For purposes of clarification, Applicants respectfully submit that the present rejection rejections claims 1-26 over the combination of Moon in view of Osada et al. Therefore, Applicants proceed under the assumption that Moon (the primary reference) is modified by Osada et al. (the secondary reference) in the present combination.

Assuming *arguendo* that Osada et al. teaches "how to eliminate residual images by applying a voltage level for turning off the TFT transistors [of Moon] upon power on,"

Applicants respectfully submit Osada et al. fails to cure the deficiencies of Moon with respect to what is actually claimed in at least claims 1, 9, 11, 19.

Moreover, Applicants respectfully submit that there is no motivation or suggestion to modify Moon with Osada et al. to "to achieve a display device wherein undesirable images appearing on a display screen are made invisible upon power on," as asserted by the Examiner. Specifically, as the Examiner is no doubt aware, Moon is directed to a screen clearing circuit for a TFT LCD and a method of clearing a TFT LCD when external power is removed from the LCD wherein residual images are eliminated, thereby improving the quality of TFT LCDs (see Moon, column 1, lines 6-11 and column 4, lines 33-36). Osada et al. discloses two alternative embodiments; the first embodiment including a display wherein residual images are eliminated upon being turned off by scanning the EL panel at least one time to eliminate electric charges stored in the pixels (see Osada et al., column 2, lines 40-51) and the second embodiment including a display wherein residual images are eliminated upon being turned on by delaying the normal display until the drive voltage reaches a predetermined level (see Osada et al., column 2, lines 52-60). Because residual images that have already been eliminated once cannot be re-eliminated, Applicants respectfully submit that there is no motivation or suggestion, either in the references themselves or in the knowledge generally available to those skilled in the art, to modify Moon (teaching wherein residual images are eliminated upon turning off a display) using Osada et al. (teaching wherein residual images are eliminated upon turning a display on).

Regardless of the propriety of the application of Moon in view of Osada et al. with respect to claims 1, 9, 11, and 19, Applicants respectfully submit that Moon fails to teach or suggest the elements as individually set forth in claims 2-8, 10, 12-18, and 20-26.

If the Examiner deems that a telephone conversation would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: April 5, 2004

Respectfully submitted,

By 4/5/06
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